IN THE UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

ACQIS LLC, a Texas limited liability company Plaintiff, v. MICROSOFT CORPORATION, a Washington corporation. Defendant.	§ § § § § § § § § §	Civil Action No. 6:22-cv-385-ADA **JURY TRIAL DEMANDED**
ACQIS LLC, a Texas limited liability company Plaintiff, v. SONY INTERACTIVE ENTERTAINMENT INC., a Japanese corporation, and SONY INTERACTIVE ENTERTAINMENT LLC, a California limited liability corporation. Defendants.	§ § § § § § § § § § §	Civil Action No. 6:22-cv-386-ADA **JURY TRIAL DEMANDED**

DEFENDANTS' CONSOLIDATED OPENING CLAIM CONSTRUCTION BRIEF

Pursuant to the Scheduling Orders of February 27, 2023, Defendants Microsoft Corporation ("Microsoft"), Sony Interactive Entertainment LLC and Sony Interactive Entertainment Inc. (collectively, "Sony") (Microsoft and Sony are collectively referred to as "Defendants") hereby submit their consolidated opening claim construction brief.[1]

[1] The identical brief is being filed in each of the cases in the above caption.

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1	U.S. Patent No. 9,529,768 ("'768 patent")
2	U.S. Patent No. 9,703,750 ("'750 patent")
3	U.S. Patent No. 8,977,797 ("'797 patent")
4	U.S. Patent No. RE44,654 ("'654 patent")
5	U.S. Patent No. RE45,140 ("'140 patent")
6	U.S. Patent No. 7,363,416
7	U.S. Patent No. 7,676,624
8	U.S. Patent No. 7,818,487
9	U.S. Patent No. RE41,294
10	U.S. Patent No. 8,041,873
11	U.S. Patent No. RE41,294
12	U.S. Patent No. RE41,961
13	U.S. Patent No. RE42,814
14	U.S. Patent No. RE42,984
15	U.S. Patent No. RE43,119
16	U.S. Patent No. RE43,171
17	U.S. Patent No. RE44,468
18	*ACQIS LLC v. ASUSTek Computer, Inc.*, 6:20-cv-966-ADA, Dkt. 64
19	*ACQIS LLC v. ASUSTek Computer, Inc.*, 6:20-cv-966-ADA, Dkt. 70
20	Declaration of Andrew Wolfe, Ph.D
21	*ACQIS LLC v. Samsung Elecs. Co*., No. 2:20-cv-00295-JRG (E.D. Tex. Sept. 26, 2021), Dkt. 92
22	"Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, TIA/EIA Standard, TIA/EIA-644 (Mar. 1996) ("*TIA/EIA-644*")
23	"IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)," IEEE Standards Board (March 21, 1996) ("*IEEE 1596.3*")
24	"National Semiconductor LVDS Owner's Manual," (1st Edition Spring 1997)
25	"National Semiconductor LVDS Owner's Manual," (2nd Ed. Spring 2000)
26	Huq, S., et al., "An Overview of LVDS Technology," Application Note 971 (Jul. 1998)
27	*ACQIS LLC v. Alcatel-Lucent USA Inc., et al*. (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129

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28	*ACQIS LLC v. Alcatel-Lucent USA Inc., et al*. (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129-15 (Ex. N)
29	*ACQIS LLC v. Alcatel-Lucent USA Inc., et al*. (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129-14 (Ex. M)
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33	Patent Owner's Preliminary Response, IPR2014-01462 ('873 Patent), Paper 11 (December 15, 2014)
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35	Institution Decision, IPR2014-01462 ('873 Patent), Paper 11 (March 11, 2015)
36	Excerpts from Hearing Transcript, IPR2014-01462; IPR2014-01469 (December 8, 2015)
37	Declaration of Robert Colwell, Ph.D
38	*ACQIS LLC v. EMC Corp.*, No. 1:14-cv-13560, Dkt. 185 (EMC Opening CC Brief)
39	Dep. Tr. of V. Lindenstruth Vol. 1 (EMC v. Acqis), IPR2014-01462, Exhibit 1028
40	ACQIS Preliminary Proposed Claim Constructions in *ACQIS LLC v. Sony Interactive Entertainment, LLC, et al*. 6:22-cv-00386-ADA
41	*ACQIS LLC v. ASUSTek Computer, Inc.*, 6:20-cv-966-ADA, Dkt. 144 (Order Memorializing Whether Prior Constructions Apply to Terms in this Case)
42	Patent Owner's Response, IPR2014-01469 ('814 Patent), Paper 25 (September 25, 2014)
43	IPR Decl. of V. Lindenstruth, IPR2014-01462 ('873 Patent), Ex. 2021 (EMC v. ACQIS)
44	Patent Owner's Response, IPR2014-01462 ('873 Patent), Paper 30 (September 25, 2014)
45	PCI Local Bus Specification, Revision 2.2 (Dec. 18, 1998)
46	Universal Serial Bus Specification, Revision 2.0 (Apr. 27, 2000)
47	U.S. Patent No. 6,718,415

I. INTRODUCTION

ACQIS accuses Microsoft of infringing more than 50 claims spanning five patents—U.S. Patent Nos. 9,529,768 ("'768 patent"), 9,703,750 ("'750 patent"), 8,977,797 ("'797 patent"), RE44,654 ("'654 patent") and RE45,140 ("'140 patent") (collectively, the "Asserted Patents"). Exs. 1-5. ACQIS accuses Sony of infringing 30 of the same claims and one additional claim. The Federal Circuit has already "specifically adopt[ed]" Defendants' proposed constructions of three disputed PCI terms. *ACQIS, LLC v. EMC Corp.,* 2022 WL 1562847 (Fed. Cir. 2022) ("*EMC Fed. Cir. Op.*"). ACQIS seeks to avoid the Federal Circuit's constructions by rewriting history. This is not permissible under the law or in view of the intrinsic evidence. With respect to the remaining terms, ACQIS seeks to modify constructions that it agreed to adopt in prior cases or that other courts construed consistent with Defendants' proposed constructions. Because Defendants' proposed constructions are supported by the intrinsic evidence and follow the Federal Circuit, the Court should adopt them.

II. ACQIS IS PRECLUDED FROM RE-LITIGATING THE *EMC* CONSTRUCTIONS

The *EMC* district court construed the three PCI terms at issue here as follows:

EMC PCI Term	EMC Construction
Peripheral Component Interconnect (PCI) bus transaction	a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component
encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction and related terms	a PCI bus transaction that has been serialized from a parallel form
communicating . . . PCI bus transaction	communicating a PCI bus transaction, including all address, data, and control bits

ACQIS, LLC v. EMC Corp., 2017 WL 6211051 (D. Mass. Dec. 8, 2017) ("*EMC Markman*"), at *5, 8. These constructions were affirmed and "specifically adopt[ed]" by the Federal Circuit. *EMC Fed. Cir. Op.* at *1. ACQIS is precluded from pursuing different constructions of the same terms

in this case as a result.

Issue preclusion, or collateral estoppel, serves to prevent parties from relitigating issues they litigated and lost in another action. *Parklane Hosiery*, 439 U.S. 322, 327 (1979). It "treat[s] specific issues of law or fact that are validly and necessarily determined between two parties as final and conclusive." *United States v. Shanbaum*, 10 F.3d 305, 311 (5th Cir. 1994). To apply, the following three elements must be met: "(1) the issue at stake must be identical to the one involved in the prior action; (2) the issue must have been actually litigated in the prior action; and (3) the determination of the issue in the prior action must have been a necessary part of the judgment in that earlier action." *RecoverEdge L.P. v. Pentecost*, 44 F.3d 1284, 1290 (5th Cir. 1995). Implicit in element three is the requirement for a final judgment. *See Int'l Union of Operating Eng'rs, Local No. 714 v. Sullivan Transfer, Inc*., 650 F.2d 669, 676 (5th Cir. 1981).

Where, as here, a party requests the Court to apply issue preclusion for defensive purposes— *i.e.*, to estop a plaintiff from asserting a claim that the plaintiff had previously litigated and lost against another defendant—the issue is a question of law. *See Bradberry v. Jefferson County, Tex*., 732 F.3d 540, 549 (5th Cir. 2013) ("the issue of whether to apply collateral estoppel is a question of law, making [the court's] review de novo," whereas abuse of discretion review applies only "when considering a district court's evaluation of whether special circumstances exist to justify offensive collateral estoppel"); *see also Parklane Hosiery*, 439 U.S. at 330-31 (distinguishing defensive collateral estoppel from offensive collateral estoppel). Thus, "[c]ollateral estoppel will apply in a second proceeding that involves separate claims if the claims involve the same issue, *Midwest Mech. Contractors, Inc. v. Commonwealth Constr. Co*., 801 F.2d 748, 751 (5th Cir. 1986), and the subject matter of the suits may be different as long as the requirements for collateral estoppel are met." *RecoverEdge*, 44 F.3d at 1291.

ACQIS "litigated and lost" the construction of the "PCI bus transaction" terms above in *EMC*, which is the subject of a final judgment, and ACQIS is precluded from pursuing different constructions of the same terms in this case. *See Parklane Hosiery*, 439 U.S. at 327.

First, the issue in this case is identical to the issue in *EMC*, namely, the construction of the "PCI bus transaction" and "encoded" terms. *See RecoverEdge*, 44 F.3d at 1290. The patents in *EMC*[2] and here are extremely similar and very closely related. The '654 and '140 patents share a specification with RE42,984, RE43,171, and RE44,468 from *EMC* as all are reissues of U.S. Patent No. 6,643,777.[3] The '768, '750 and '797 patents share a specification with U.S. Patent Nos. 7,363,416, 7,676,624, 7,818,487 and 8,041,873 from *EMC*, and all are continuations of U.S. patent application no. 09/569,758.[4] All of the patents share the same inventor and subject matter.

The extremely close relationship of the Asserted Patents and claim language shared between the patents warrants the same construction of "PCI bus transaction," "encoded"/ "PCI bus transaction" / "serial," and "communicating a PCI bus transaction"—making the issues identical for collateral estoppel purposes. *See, e.g., In re Rambus Inc.*, 694 F.3d 42, 48 (Fed. Cir. 2012) (quoting *Omega Eng'g, Inc. v. Raytek Corp*., 334 F.3d 1314, 1334 (Fed. Cir. 203)) ("The same claim term in the same patent or related patents carries the same construed meaning."); *SightSound Techs., LLC v. Apple Inc*., 809 F.3 1307, 1316 (Fed. Cir. 2015) ("Where multiple patents 'derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents; *Abtox, Inc. v. Exitron Corp*., 131 F.3d 1009, 1010 (Fed. Cir. 1997 ("Although these claims have since issued in separate patents, it would be improper to

[2] U.S. Patent Nos. 7,363,416; 7,676,624; 7,818,487; 8,041,873; RE41,294; RE41,961; RE42,814; RE42,984; RE43,119; RE43,171; and RE44,468. Exs. 6-17.

[3] The '654 and '140 patents are continuations of RE42,984 and RE44,468.

[4] The '768, '750 and '797 patents are continuations of U.S. Patent No. 8,041,873.

construe this term differently in one patent than another, given their common ancestry.").

For example, claim 38 of U.S. Patent No. 7,818,487, asserted in *EMC* (*see ACQIS, LLC v. EMC Corp.*, No. 14-cv-13560, 2021 WL 1088207, at *1, 3-4 (D. Mass. Feb. 19, 2021) ("*EMC MSJ*")), includes a low voltage differential signal ("LVDS") with two unidirectional, serial channels for transmitting encoded PCI bus transaction data in opposite directions. Ex. 8 at 40:44-48 (claim 38 depends on claim 36). Here, claim 7 of the '797 patent similarly claims an "LVDS channel comprising two unidirectional, serial channels that transmit data in opposite directions" and "conveying encoded address and data bits of a Peripheral Component Interface (PCI) bus transaction in serial form over the serial channels." Ex. 3 at 38:45-49, 38:53-56. The Court should construe such highly similar claims consistently across the patents. *In re Katz*, 639 F.3d at 1325; *SightSound*, 809 F.3d at 1316. It does not matter that some of the patent claims themselves are not identical so long as the issues litigated are the same—*i.e.*, construction of "PCI bus transaction," "encoded" / "PCI bus transaction" / "serial," and "communicating a PCI bus transaction." *See, e.g., Ohio Willow Wood Co. v. Alps South LLC*, 735 F.3d 1333, 1342 (Fed. Cir. 2013) ("Our precedent does not limit collateral estoppel to patent claims that are identical. Rather, it is the identity of the issues that were litigated that determines whether collateral estoppel should apply."); *Sprint Commc'ns Co. L.P. v. Cequel Commc'ns, LLC*, No. 18- cv-1919, 2020 WL 3048175, at *3 (D. Del. June 8, 2020).

***Second*,** the issue was actually litigated in the *EMC* case. ACQIS and EMC fully and extensively briefed their respective claim constructions to the District of Massachusetts, the Eastern District of Texas (before transfer to Massachusetts), and the Federal Circuit, resulting in seven briefs and at least three oral arguments on proper construction of the claim terms. *See EMC Markman* and *ACQIS LLC v. Alcatel-Lucent USA Inc.*, No. 6:13-cv-638, 2015 WL 1737853 (E.D.

Tex. Apr. 13, 2015) ("*EDTX Markman*") (discussing briefing); *see also EMC Fed. Cir. Op.*; Ex. 18, *ACQIS LLC v. ASUSTek Computer, Inc.*, 6:20-cv-966-ADA, Dkt. 64 at 7-9 (detailing history), Ex. 19, Dkt. 70 at 4-7.

Third, determination of these terms' constructions was necessary to support the final judgment in *EMC*. The District of Massachusetts granted summary judgment of non-infringement on the basis that the accused products did not contain a "PCI bus transaction" as construed, and did not contain a parallel-to-serial conversion. *EMC SJ Order,* 2021 WL 1088207, at *3, *5 ("Accordingly, because the accused products do not contain the limitations set forth in the asserted claims, which recite a PCI bus transaction with reference to the Specification, the Court concludes that there is no infringement and summary judgment is appropriate."), *6 ("ACQIS has not shown that EMC's accused products serialized a PCI bus transaction from parallel to serial and back to parallel."). The Federal Circuit affirmed summary judgment and "specifically adopt[ed]" the district court's constructions. *EMC Fed. Cir. Op.*, 2022 WL 1562847, at *1.

Accordingly, the Court should not modify the *EMC* constructions, which are subject to a final judgment affirmed by the Federal Circuit.

III. DISPUTED CLAIM TERMS

A. "low voltage differential signal (LVDS) [channel]" / "LVDS [channel]"

'797 patent: 7, 14, 33-34, 36; '768 patent: 1, 2, 4, 13, 17, 39-40; '750 patent: 1-2, 5, 7, 10, 12, 21, 24, 31, 34-35, 44; '654 patent: 20, 21, 23, 26, 35; '140 patent: 14-15, 17-19, 21, 30-31, 34-36, 38.	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"[a channel for carrying] a signal in accordance with ANSI/TIA/EIA-644 or IEEE 1596.3" or, alternatively, indefinite.	No construction necessary. These terms should be given their plain and ordinary meaning.

Each of the Asserted Claims require one or more "low voltage differential signal (LVDS)" channels over which, in certain instances, specific types of data are conveyed.

The phrase "low voltage differential signal (LVDS)" relates to well-known technology defined by the standards recited in Defendants' proposal and should be construed accordingly. *See* Ex. 20 (*Wolfe Decl.*), ¶¶ 27-28. This is because the relevant meaning of "LVDS" – a standard-based technology – is the meaning when the inventor filed the earliest related patent application. *BillJCo, LLC v. Cisco Sys., Inc.*, No. 2:21-CV-00181-JRG, 2022 WL 782740, at *5 (E.D. Tex. Mar. 14, 2022) (agreeing that "a Bluetooth communications interface" means "a communications interface using Bluetooth ***standards that existed at the time of the claimed invention***"[5]); Ex. 21, *ACQIS LLC v. Samsung Elecs. Co*., No. 2:20-cv-00295-JRG (E.D. Tex. Sept. 26, 2021), Dkt. 92 at 32-33 (stating "the term 'Universal Serial Bus (USB) protocol' must be ***interpreted as of the priority date***"); *Fundamental Innovation Sys. Int'l LLC v. Samsung Elecs. Co.*, Case No. 2:17-cv-145-JRG-RSP, 2018 WL 647734, at *11 (E.D. Tex. Jan. 31, 2018) (citation omitted) ("[T]he term 'USB' in the patents-in-suit should be limited to the Universal Serial Bus ***standards that existed at the time of the claimed invention***."); *Uniloc USA, Inc. v. Apple, Inc*., No. 19-cv-1692, 2021 WL 432183, at *8 (N.D. Cal. Jan. 15, 2021) (report and recommendation finding that terms "Bluetooth messaging" and "Bluetooth protocols" should be limited to functionality described in the Bluetooth Core Specification "***as it existed at the time of the claimed invention***").

Here, the two reissue Asserted Patents (the '654 and '140 patents) both trace back to a patent application filed on May 14, 1999. Exs. 4 and 5, Patent Covers at (64). The earliest application for the three non-reissue Asserted Patents (the '768, '750 and '797 patents) was filed on May 14, 1999, and the earliest non-provisional application was filed on May 12, 2000. Ex. 1-3, Patent Covers at (63). Thus, the relevant meaning of the LVDS claim terms is the meaning they had as of May 14, 1999, or May 12, 2000 at the latest. *Fundamental Innovation*, 2018 WL 647734,

[5] All emphases are added unless noted otherwise.

at *9 ("An invention cannot comply with standards not yet in existence.").

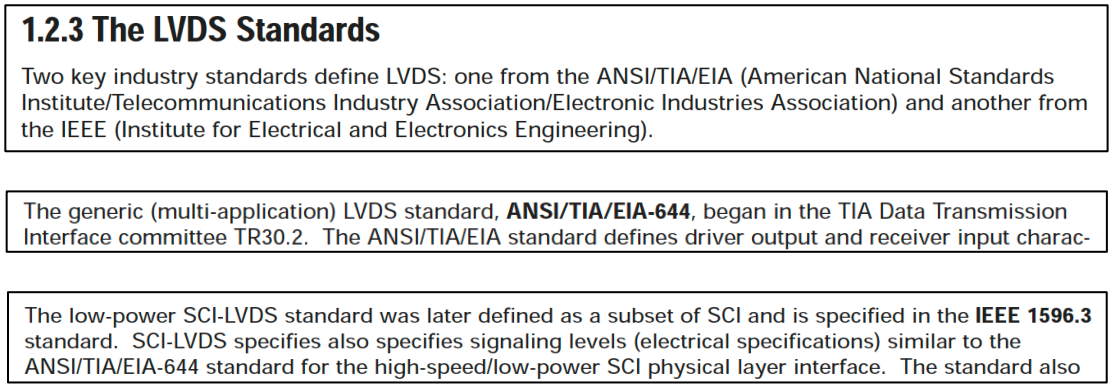
As of May 12, 2000, LVDS was well-known to a POSITA to refer to the standards in place at the time—ANSI/TIA/EIA-644 or IEEE 1596.3. Ex. 20 (Wolfe Decl.), ¶¶ 27-28. Thus, a POSITA would have understood that the Asserted Patents' reference to "LVDS" means "a signal in accordance with" at least one of these standards. *Id*., ¶¶ 27-37.[6]

Defendants' construction is confirmed by the intrinsic evidence. The inventor cited numerous documents discussing the LVDS standards recited in Defendants' construction during prosecution of the Asserted Patents. Indeed, the '750 and '768 patents specifically identify the ANSI/TIA/EIA-644 LVDS standard in the References Cited. Ex. 2, '750 patent at Page 6 (References Cited) (identifying "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, TIA/EIA Standard, TIA/EIA-644, Mar. 1996, 42 pages"); Ex. 1, '768 patent at Page 6 (References Cited) (identifying same); *see also* Ex. 22, ANSI/TIA/EIA-644 LVDS Standard ("*TIA/EIA-644*"). The TIA/EIA-644 LVDS Standard "specifies the electrical characteristics of low voltage differential signaling interface circuits." *TIA/EIA-644* at p. 1; *see also id.* at v (Foreword). For example, each of the standards defines an output differential voltage, or voltage swing, in the range of 247 to 454 mV. Ex. 22, *ANSI/TIA/EIA-644* at Foreword ("The low voltage (330 mV) swing limits power dissipation, while also reducing radiation of EMI signals."), p. 8 ("the steady-state magnitude of the differential output voltage (Vt), shall be greater than or equal to 247 mV … and less than or equal to 454 mV"); Ex. 23, *IEEE 1596.3* Standard at Abstract ("IEEE Std 1596.3-1996, an extension to IEEE Std 1596-1992, defines a lower-voltage differential signal (as low as 250 mV swing) that is compatible with low-voltage CMOS, BiCMOS,

[6] This is no different than the Court's requirement that a "PCI bus transaction" be "in accordance … with the industry standard PCI Local Bus Specification" (i.e., the PCI Local Bus Specification in effect at the time of the invention).

and GaAs circuitry."), 2 ("The basic design strategies selected by this standard include the following: -- *Low-voltage swing*. To minimize power dissipation and enable operation at very high-speed, low-swing (400 mV maximum) signals are specified."), 7 (defining range for output differential voltage (Vod) as between 250 and 450 mV). The TIA/EIA-644 LVDS Standard also specifically recognizes the other standard in Defendants' construction, IEEE 1596.3. Ex. 22, *ANSI/TIA/EIA-644* at p. v ("The dc electrical levels are similar to electrical levels described in the IEEE 1596.3 standard[.]").

The '750 and 768 patents also identify additional intrinsic evidence that support Defendants' proposed construction. The first document, "LVDS Owner's Manual," recognizes that ***"[t]wo key industry standards define LVDS***"—ANSI/TIA/EIA-644 and IEEE 1596.3:



1.2.3 The LVDS Standards

Two key industry standards define LVDS: one from the ANSI/TIA/EIA (American National Standards Institute/Telecommunications Industry Association/Electronic Industries Association) and another from the IEEE (Institute for Electrical and Electronics Engineering).

The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input charac-

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the **IEEE 1596.3** standard. SCI-LVDS specifies also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also

Ex. 24, "National Semiconductor LVDS Owner's Manual," (1st Edition Spring 1997), at 2-3 ((cited by '750 patent and '768 patents at Page 9 (References Cited)); *see also* Ex. 25, "National Semiconductor LVDS Owner's Manual," (2nd Ed. Spring 2000), at 1 (stating "LVDS is currently standardized by two different standards: [ANSI/TIA/EIA-644 and IEEE 1596.3]") ((cited by '750 patent and '768 patents at Page 12 (References Cited)).

"An Overview of LVDS Technology," also included in the References Cited, states:

> "***There are two industry standards that define LVDS***. The more common of the two is the generic electrical layer standard defined by the TIA. This standard is know[n] as ***ANSI/TIA/EIA-644***. The other application specific standard is an IEEE

… standard titled ***Scalable Coherent Interface (SCI)***."

Ex. 26, Huq, S., et al., "An Overview of LVDS Technology," Application Note 971, Jul. 1998, at 1 (describing ANSI/TIA/EIA-644 and "IEEE 1596.3 SCI-LVDS") (cited by '750 patent at Page 6 (References Cited) and '768 patent at Page 6 (References Cited)). The *Overview of LVDS* explains that "[a]s the name implies, LVDS features a low voltage swing compared to other industry data transmission standards." *Id.* at 1.

ACQIS relied on this same LVDS Owner's Manual in prior litigation to argue "LVDS is a term of art used to describe a type of signaling that was well-known" and "embodied in numerous standards and applications at the time of the invention." Ex. 27, *ACQIS LLC v. Alcatel-Lucent USA Inc., et al*. (ACQIS Opening CC Brief), No. 6:13-cv-638, Dkt. 129 at 7-8; Ex. 28 (Ex. N from ACQIS brief). Specifically, ACQIS argued that "the Patents-in-Suit cite to several prior art references ***that define LVDS, and illustrate the meaning of the term as it was generally used at the time of the inventions***," pointing to "An Overview of LVDS Technology" and the ANSI/TIA/EIA-644 standard. *Id*. at 8 (citing Ex. 29 (Ex. M from ACQIS brief)). "These references," according to ACQIS, "confirm that LVDS was a well-known and readily understood term." *Id.*

In that same brief, ACQIS relied on extrinsic evidence that supports Defendants' proposed construction. *Id*. at 8. In *Interface Circuits for TIA/EIA-644 (LVDS)*, TIA/EIA-644 and LVDS are treated as one and the same. Ex. 30 (Ex. O from ACQIS brief), Texas Instruments, *Interface Circuits for TIA/EIA-644 (LVDS)*, at 1 (Sept. 2002) ("***TIA/EIA-644, otherwise known as LVDS***, is a signaling method used for high-speed, low-power transmission of binary data over copper."). Defendants' construction is supported by additional extrinsic evidence. *See* Ex. 31, Ma, J., "A Closer Look at LVDS Technology," Application Note 41 at 1 (Pericom Nov. 16, 2001) ("What is

LVDS? LVDS stands for Low Voltage Differential Signaling. ***LVDS is defined in the TIA/EIA-644 standards and the IEEE 1596.3 standards***."). Accordingly, the Court should construe "LVDS [channel]" as "[a channel for carrying] a signal in accordance with ANSI/TIA/EIA-644 or IEEE 1596.3." *Mass. Inst. of Tech. v. Abacus Software*, 462 F.3d 1344, 1353 (Fed. Cir. 2006) (finding a claim term "should be defined by what was known in the art at the time").

If the Court does not adopt Defendants' construction, the phrase "low voltage differential signal" is indefinite. The phrase "low voltage differential signal," absent reference to the standards identified in Defendants' construction, is a subjective term of degree for which the claims, specification, and prosecution history of the Asserted Patents provide no objective standard or boundaries for ascertaining the scope of the term or informing a POSITA with reasonable certainty of the same. *See U.S. Well Servs., Inc. v. Halliburton Co*., No. 6:21-cv-00367-ADA, Dkt. No. 74, at 9-18 (W.D. Tex. Jan. 17, 2022) (holding the term "high pressure" to be indefinite" as an improper term of degree); *Biosig Instruments, Inc. v. Nautilus, Inc.*, 783 F.3d 1374, 1378 (Fed. Cir. 2015); *see also Nautilus, Inc. v. Biosig Instruments, Inc.,* 572 U.S. 898, 901 (2014); *Ernie Ball, Inc. v. Earvana, LLC*, 502 F. App'x 971, 980 (Fed. Cir. 2013) (noting that when a subjective term is used in a claim, "a court must determine whether the patent's specification supplies some standard for measuring the scope of the [term]"); *Wolfe Decl*., ¶¶ 38-43.

B. "Peripheral Component Interconnect (PCI) [/PCI] bus transaction"

'797 patent: 7, 14, 36, 38; '768 patent: 1-5, 13, 14, 17, 39; '750 patent: 1, 2, 3, 5, 7, 10, 12, 21, 31-35, 44, 45; '654 patent: 21, 24, 26, 35; '140 patent: 30, 31, 34.	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"	"a transaction, in accordance or backwards compatible with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"

As discussed above, this claim term is subject to a final judgment of the Federal Circuit

that is identical to Defendants' construction, which should be adopted for that reason.[7] Defendants' construction also should be adopted because it is consistent with intrinsic evidence and does not inject uncertainty into these proceedings. By contrast, ACQIS's construction improperly attempts to inject unsupported ambiguity through the addition of "or backwards compatible"—words never used in the intrinsic evidence.

1. ACQIS's Proposed Construction Injects Unnecessary and Unsupported Ambiguity

The Federal Circuit limited "PCI bus transaction" to a single category of transactions—transactions "in accordance with the industry standard PCI Local Bus Specification." *EMC Markman*, at *3-5; *EMC Fed. Cir. Op.*, 2022 WL 1562847 (specifically adopting same). ACQIS's proposed modification is simply not the same words as the Federal Circuit's construction. Instead, it adds language that is neither necessary, nor supported by the specification.

ACQIS presumably intends to use this injected ambiguity to wrongly attempt to continue infringement claims against devices using PCIe. But ACQIS's theory has already been rejected by the *EMC* district court and the Federal Circuit. *EMC MSJ,* 2021 WL 1088207*; EMC Fed. Cir. Op.*, 2022 WL 1562847. The *EMC* court and the Federal Circuit held that transactions in accordance with the PCIe standards could not satisfy the claimed "PCI bus transaction," as construed. *EMC MSJ,* 2021 WL 1088207, at *3-6*; EMC Fed. Cir. Op.*, 2022 WL 1562847. ACQIS's attempt to modify the construction contradicts the Federal Circuit's final judgment on claim construction (and

[7] It is worth noting that ACQIS previously agreed to the substance of Defendants' proposed construction. *EMC Markman*, 2017 WL 6211051, at *3; *EMC MSJ*, 2021 WL 1088207, at *3. The parties' only dispute in *EMC* was whether a "PCI bus transaction" required a PCI bus (EMC said yes and ACQIS said no). Consistent with the Eastern District of Texas' prior ruling on this issue, the District of Massachusetts agreed that an actual PCI bus is not required by the claims. *EDTX Markman*, 2015 WL 1737853 at *4-5; *EMC Markman*, 2017 WL 6211051 at *4.

on non-infringement) in *EMC* and is not a mere clarification. Adding "or backwards compatible" improperly changes the construction of "PCI bus transaction" beyond the limits set by the Federal Circuit, which this Court may not do. *See*, *e.g.*, *Eolas Techs., Inc. v. Adobe Sys., Inc.*, No. 09-CV-446, 2011 WL 11070303, at *2 (E.D. Tex. Sept. 23, 2011) (acknowledging Federal Circuit constructions as binding). The Federal Circuit's construction is clear, and the Court should reject ACQIS's improper attempt to alter and inject confusion into that construction by adding words.

2. The Intrinsic Evidence Does Not Support "Backwards Compatible" Transactions

Adding "or backwards compatible" to the construction is not supported by, and is inconsistent with, the intrinsic evidence. For starters, the term "backwards" does not appear in any of the Asserted Patents, let alone the phrases "or backwards compatible with" or "backwards compatible" or anything equivalent. Likewise, no intrinsic evidence supports expanding the definition of a "PCI bus transaction" to include "backwards compatible" transactions that are not "in accordance with" the PCI Local Bus Specification." On the contrary, the only discussion related to "compatibility" in the intrinsic record concerns maintaining interoperability with then-existing peripheral devices through ***compliance with*** the industry standard PCI Specification. Ex. 2 ('750 patent) at 22:11-14. Accordingly, the intrinsic evidence contradicts and does not support ACQIS's construction.

3. ACQIS Previously Told Both the PTAB and the District Court that a "PCI Bus Transaction" Must in Fact Be a PCI Bus Transaction

ACQIS's proposed construction that a PCI bus transaction need only be "backwards compatible with the industry standard PCI Local Bus Specification" also flatly contradicts what ACQIS told the PTAB during the related EMC *IPR* proceedings, namely that a PCI bus transaction is a bus transaction under the PCI protocol (and not anything less). In attempting to avoid the reach of prior art, ACQIS unequivocally told the PTAB, which was then operating under the

broadest reasonable construction standard, that a "PCI bus transaction" should be limited "to a bus transaction according to [the] protocol standard." Ex. 32 ('814 IPR Prelim. Resp.) at 7; Ex. 33 ('873 IPR Prelim. Resp.) at 6 (same); *see also* Ex. 32 ('814 IPR Prelim. Resp.) at 6-10 ("The Board similarly should limit … 'PCI bus transaction' to a bus transaction according to that protocol standard."). These repeated, unequivocal statements by ACQIS clearly equated a "PCI bus transaction" with a bus transaction according to the PCI protocol. These statements are not surprising, because they align perfectly with the plain meaning of "PCI bus transaction"—a bus ***transaction*** in accordance with the PCI standard. The PTAB agreed and construed the term as a "Peripheral Component Interconnection (PCI) industry standard bus transaction." Ex. 34 ('814 IPR Institution) at 7; Ex. 35 ('873 IPR Institution) at 7.

ACQIS did not tell the PTAB that "backwards compatible" was required for a "PCI bus transaction" to maintain ACQIS's patents. ACQIS made clear that a "PCI bus transaction" was not merely a transaction compatible with the PCI standards. Instead, ACQIS made clear that adhering to the PCI standard requires communicating all address, data, and control bits, and that not doing so would "make sure [the transaction] does not comply with either the standard of a PCI or the purpose of the invention." Ex. 36 (IPR2014-01469 Hr'g Tr.) at 38:5-20; *see also id.* at 35:11-17 (ACQIS arguing PCI standard requires, *inter alia*, address bits, data bits, and control bits), 50:12-16 (same); *see also infra,* Section III.C. Thus, when ACQIS was distinguishing prior art in the IPRs, it made clear that a PCI bus transaction needs ***all the bits*** to complete the transaction (including control bits that are not included ACQIS's construction). A bus transaction requiring all the bits called for by the PCI bus specification excludes the additional class of transactions that are merely backwards compatible as ACQIS proposes. These clear statements made by ACQIS to the PTAB are important intrinsic evidence. They confirm the Court should reject ACQIS's

proposed construction, which is inaccurate and contradicts what ACQIS told the PTAB. *Aylus Networks, Inc. v. Apple Inc.*, 856 F. 3d 1353, 1360, 1362 (Fed. Cir. 2017) ("we hold that statements made by a patent owner during an IPR proceeding, whether before or after an institution decision, can be considered for claim construction . . ." and "[e]xtending the prosecution disclaimer doctrine to IPR proceedings will ensure that claims are not argued one way in order to maintain their patentability and in a different way against accused infringers").

ACQIS also agreed in *EMC*—notably, ***after*** the *IPR* proceedings were completed—that an actual PCI "transaction" is necessary by offering a construction that imposed a PCI transaction requirement. The *EMC* Court adopted ACQIS's construction with additional modifications that ACQIS agreed to accept during the *Markman* process. *EMC Markman*, 2017 WL 6211051, at *3; *EMC MSJ*, 2021 WL 1088207, at *3. This makes sense, as the claim term itself refers to a PCI transaction, and a POSITA would have understood the claim term, consistent with the intrinsic evidence, to require a PCI transaction "in accordance with the industry standard." Ex. 37 (Colwell Decl.) at ¶¶ 32-37.[8] Accordingly, the Court should adopt Defendants' construction.

C. <u>"convey [/conveying/conveys/communicating/communicate/transmitting] … a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]"</u>

'797 patent: 7, 14, 36, 38; '768 patent: 1-5, 13, 14, 17, 39; '750 patent: 1, 2-3, 5, 7, 10, 12, 21, 31-35, 44-45; '654 patent: 21, 24, 26, 35; '140 patent: 30, 31, 34.	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"communicating a PCI bus transaction, including all address, data, and control bits"	"[Peripheral Component Interconnect (PCI)/PCI] bus transaction": See proposed construction of PCI Bus Transaction Terms. Remaining portions of these phrases do not require construction.

[8] When ACQIS later attempted to backtrack on its prior position in the face of EMC's summary judgment motion, the *EMC* Court stated "[t]here is no need to now construe a readily understandable term that ACQIS itself thought clear when offering proposed constructions of related terms and the Court will not do so." *EMC MSJ*, 2021 WL 1088207, at *5.

In addition to generating and serializing a PCI bus transaction, the claims require "conveying," "communicating," or "transmitting" that PCI bus transaction. But it is not enough to communicate *some*—or even *most*—bits of a PCI bus transaction. Rather, as one district court explained in a prior claim construction order, "a PCI bus transaction must include ***all*** information required by the PCI standard." *EDTX* Markman, 2015 WL 1737853, at *5.

As discussed above in Section II, Defendants maintain that ACQIS is precluded from arguing for a construction of this claim limitation different than the construction of the same term affirmed by the Federal Circuit. The Court should adopt Defendants' construction for four additional reasons. ***First***, ACQIS agreed to this exact construction of the same term in *EMC*, despite the fact that certain claims recited "address and data" of a PCI bus transaction. Ex. 38, *ACQIS LLC v. EMC Corp.*, No. 1:14-cv-13560, Dkt. 185 (EMC Opening CC Brief), at 21 (identifying exemplary claim language including "address and data bits of PCI bus transaction" and "[PCI] bus transaction address and data"); *EMC Markman*, 2017 WL 6211051, at *8. ACQIS's agreed construction was adopted by the district court and affirmed by the Federal Circuit. This should end the inquiry.

Second, Defendants' construction comports with the plain language of the claims. The claims recite specific bits "of a PCI bus transaction." There can be no specific bits of a PCI bus transaction without an actual "PCI bus transaction." ACQIS seeks to read the language "of a PCI bus transaction" out of the claims because it cannot dispute that the accused products do not have PCI bus transactions. The Court should reject ACQIS's infringement-driven position.

Third, Defendants' construction is correct because it accounts for ACQIS's repeated and unequivocal disclaimers at the PTAB. During the IPRs, ACQIS repeatedly and unambiguously represented (again, in distinguishing prior art to survive the IPRs) that the claims require

communicating *all* (not just some) bits of a PCI bus transaction required under the PCI Local Bus Specification. Ex. 36, IPR Hr'g Tr. at 35:11-17, 50:12-16. In doing so, ACQIS disclaimed anything less than a full PCI bus transaction under the PCI Local Bus Specification, including all address, data, and control bits. ACQIS did so for claims that recite conveying a PCI bus transaction and even those that recite conveying specific bits of a PCI bus transaction. Whether the claims reference specific bits or not, ACQIS's repeated statements to the PTAB expressly disclaimed the broad construction that ACQIS now seeks in this case.

Specifically, ACQIS's counsel repeatedly told the PTAB that to comply with the PCI Local Bus Specification, all portions of the PCI bus transaction needed to be transmitted, including the control bits:

- "[I]f you look at the standard, there are three types of information included in every PCI transaction. Three types. There's an ***address, there's data and then there's control***. That's straight out of the standard. ***You have those three things***." Ex. 36 (IPR Hr'g Tr.), at 35:13-17.
- "[Claim] Fifty-four requires the encoded serial bit stream of peripheral component Internet [sic] connect bus transaction. That includes the ***information necessary to make a PCI transaction under the defined standard***. ***That includes data***, ***that includes address*** except for the interrupt acknowledge, and ***that includes the control bits every time***. So you didn't hear a word about control bits, period. There is no such thing -- just put it bluntly, ***there is no such thing as a PCI transaction that does not have control bits***. To carve control bits out of claim 54 and 61 is to make sure it does not comply with either the standard of a PCI or the purpose of the invention." *Id*. at 38:7-17.
- "So when we talk about [claim] 54, ***you have to talk about control bits***. And not once do they talk about Horst or Bogaerts transmitting any type of control bits. Just doesn't happen." *Id*. at 38:18-20.
- "[C]laim 54 ***requires a PCI transaction. Got to have control bits***." *Id*. at 49:13-14.
- "[W]hat that claim requires is that it is a ***PCI bus transaction. That is defined by the standard. You know the three portions: Address, data and control***." *Id*. at 50:14-16.

ACQIS's IPR expert likewise explained that the control bits "define the transaction" and "have to be there" in his deposition. Ex. 39 (V. Lindenstruth Dep. Tr.), at 145:18-146:17. When asked whether a claim that recited "address and data bits of PCI transaction in serial form" required the non-recited "command information," he explained that despite "explicitly" reciting only

"address and data bits," the claim still requires any "other corollary information which is needed to define a PCI transaction." *Id*. at 121:5-8, 121:13-17 ("It doesn't say explicitly the other corollary information which is needed to define a PCI transaction, but it says "PCI transaction". So without, for instance, the additional functionality, it wouldn't be a PCI transaction."). Dr. Lindenstruth clarified that the PCI control lines were "corollary signals which basically define what's going on[.]" *Id*. at 142:17-143:6; *see also id*. at 145:18-146:17 (stating control lines "define the PCI transaction, so have to be there").

ACQIS's "repeated and unqualified statements" mean "the interested public is entitled to conclude that the claimed devices and methods" of the claims require that a PCI bus transaction must include all the portions required by the PCI Local Bus Specification, including control bits. *See, e.g., Gammino v. Sprint Commc'ns Co., L.P*., 577 F. App'x 982, 989 (Fed. Cir. 2014).

ACQIS cannot avoid this outcome on the basis that the claims specifically recite "address bits," "data bits," or "byte enable information." This is because claim 54 of the '873 patent at issue in the IPR did not recite any specific bits, while claim 61 of the '873 patent (which depends from claim 54 and was also at issue) and claim 24 of the '814 patent (from the related proceeding) both recited "address and data bits." Given this fact, ACQIS's counsel still repeatedly and consistently argued that a PCI bus transaction requires address, data, and control bits. Indeed, this specific issue was in dispute in the IPR. When EMC's counsel raised the issue by arguing that claim 54 was broader than claim 61 and could include things other than address and control bits, ACQIS resisted, arguing that there is "an import thing here about [claim] 61 …. There's an address, there's data and then there's control. That's straight out of the standard. You have those three things." Ex. 36 (IPR Hr'g Tr.), at 35:13-17; *see also id*. at 14:20-21; 19:22-20:3. In distinguishing the prior art, ACQIS explained that "to carve control bits out of claim 54," which only recited a PCI bus

transaction, "is to make sure it does not comply with either the standard or the purpose of the invention." *Id*. at 38:9-17. ACQIS's effort to advance an argument here that it rebutted in the IPRs is disingenuous. In any event, by virtue of its arguments to overcome prior art, ACQIS has forever surrendered the broad claim scope that it now seeks. *Springs Window Fashions*, 323 F.3d at 993.

Finally, Defendants' construction also is supported by the specifications of the Asserted Patents, which show control bits being part of the PCI bus transaction. *See, e.g.*, '750 Patent at Figs. 13 and 14 (both showing bits BS0-BS3, which include control signals FRAME#, IRDY#, and TRDY#, as part of PCI bus transaction); 21:53-56; 22:29-30. There is not a single embodiment in any of the patents that shows communicating a PCI bus transaction without communicating the address, data, and control bits. Rather, *every embodiment* discloses communicating *all* the address, data, and control bits—which is strong evidence that the claims should be construed accordingly. *See In re Abbott*, 696 F.3d at 1149. Accordingly, the Court should adopt Defendants' construction.

D. "of a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]"

'797 patent: 7, 14, 36, 38; '768 patent: 1-5, 13, 14, 17, 39; '750 patent: 1-3, 5, 7, 10, 12, 21 31-35, 44, 45; '654 patent: 21, 24, 26, 35; '140 patent: 30-31, 34.	
Defendant Microsoft's Proposed Construction	**Plaintiff's Proposed Construction**
"from a transaction that is in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"	"[Peripheral Component Interconnect (PCI)/PCI] bus transaction": See proposed construction of PCI Bus Transaction Terms. Remaining portions of these phrases do not require construction.

The terms "of a Peripheral Component Interconnect (PCI) bus transaction" and "of a PCI bus transaction" (hereinafter the "Of PCI" term) are recited in conjunction with certain information in various claims of the Asserted Patents, with "address and data bits," or "address bits, data bits, and byte enable information bits," or "address and data" preceding the Of PCI term. In each case,

certain information such as address, address bits, data, data bits, and/or byte enable information bits (hereinafter "address/data") "of a [Peripheral Component Interconnect (PCI)] / [PCI bus transaction]" is recited. In some of these claims, the Of PCI term is recited along with "encoded" (e.g., the address/data is encoded) and/or "serial" (e.g., the address/data is conveyed in serial form). *See* '797 patent, claims 1, 4, 7, 10, 14, 18, 21, 36; '768 patent, claims 1, 4, 18, 22, 27, 30, 39; '750 patent, claims 5, 10, 14, 18, 21, 27, 35, 44, 46; '654 patent, claims 14, 17, 26, 35. In other claims, the Of PCI term is recited along with "encoded" but not "serial." *See* '768 patent, claims 33, 37. In yet other claims, the Of PCI term is recited along with "serial" but not "encoded." See '768 patent, claims 1, 10, 13, 15; '750 patent, claims 1, 25, 29, 31.

These claims, or claims that depend thereon, further recite preserving, conveying, or transmitting "the PCI bus transaction" as follows:

- "to preserve ***the PCI bus transaction***" (See '797 patent, claims 1, 4, 7, 10, 14, 18, 21; '654 patent, claims 14, 17, 26, 35.)
- "conveying ***the encoded PCI bus transaction***" (See '797 patent, claims 18, 21.)
- "convey[s]/[transmit] ***the PCI bus transaction***" (See '797 patent, claims 36; '768 patent, claims 1-6, 11-12, 14, 16-21, 23-25, 28-29, 31-33, 35, 38-39; '750 patent, claims 2-3, 6, 11, 16-17, 19, 22-23, 26, 28, 30, 32-33, 37-38, 45, 47.)
- "enabling ***the PCI bus transaction*** to be conveyed" (See '654 patent, claims 14, 17.)

The language reciting that "the PCI bus transaction" be preserved, conveyed or transmitted unequivocally requires that there be a PCI bus transaction, otherwise the PCI bus transaction could not be preserved, conveyed or transmitted. However, in <u>all</u> instances, there is no prior recitation of or reference to a PCI bus transaction ***other than the Of PCI term***. The Of PCI term is the ***sole*** antecedent basis for "the PCI bus transaction" in all instances where it is recited as being preserved, conveyed or transmitted. This logically means that the address/data of the Of PCI term must be from a PCI bus transaction, namely the recited "the PCI bus transaction," so that "the PCI bus transaction" can be preserved, conveyed or transmitted as recited in the claims.

Moreover, the address/data being from a PCI bus transaction is NOT dependent on whether the Of PCI term is combined with "encoded" and/or "serial." This is made explicitly clear by the various claims of the Asserted Patents, because all three possible combinations are claimed (i.e. encoded alone, serial alone, both encoded and serial), and each of the three possible combinations separately provides the sole antecedent basis support for "the PCI bus transaction" being preserved, conveyed or transmitted. Specifically, claims combining the Of PCI term with "encoded" and/or "serial" provide the sole antecedent basis support for "the PCI bus transaction." *See* '797 patent, claims 1, 4, 7, 10, 14, 18, 21, 36; '768 patent, claims 1, 4, 10, 13, 15, 18, 22, 27, 30, 33, 37, 39; '750 patent, claims 1, 5, 10, 14, 18, 21, 25, 27, 29, 31, 35, 44, 46; '654 patent, claims 14, 17, 26, 35. Therefore, the meaning of the Of PCI term does not change with respect to the origins of the address/data depending upon whether "encoded" and/or "serial" are additionally recited.

In fact, there are many instances where the claims recite conveying the address/data of a PCI bus transaction "to preserve the PCI bus transaction" together in the same claim phrase. *See* '797 patent, claims 1, 4, 7, 10, 14, 18, 21; '654 patent, claims 14, 17, 26, 35. The plain language of the claims makes clear that the claimed address/data "of a PCI bus transaction" must be from a PCI bus transaction, or else the recitation to preserving the PCI bus transaction is rendered meaningless.

ACQIS's plain and ordinary meaning may improperly allow these claim terms to be met if the address/data recited with the Of PCI term simply meet some minimal portions of the PCI Local Bus Specification, irrespective of their source. That cannot be the case, because a PCI bus transaction cannot be preserved, conveyed or transmitted as recited by the claims merely by sending random address/data that happen to meet some portion of the PCI Local Bus Specification.

The address/data recited in combination with the Of PCI term must be ***from*** a PCI bus transaction so that the PCI bus transaction can be preserved, conveyed or transmitted as claimed.

The '140 patent claims do not recite preserving, conveying or transmitting "the PCI bus transaction." However, the claims of the '140 patent do recite the Of PCI term in combination with address/data. Given that the specification of the '140 patent is identical to the specification of the '654 patent, there is no basis to interpret the Of PCI term differently in the '140 patent relative to the other Asserted Patents. *In re Rambus Inc.*, 694 F.3d at 48; *Omega Eng'g,* 334 F.3d at 1334.

E. Claims reciting a [Peripheral Component Interconnect] PCI bus transaction, or an encoded [Peripheral Component Interconnect] PCI bus transaction, "in [a] serial form" or "serially encoded" or "in a serial bit stream"

'797 claims 7, 14, 36; '768 claims 1, 2, 4, 13, 17, 39; '750 claims 1, 2, 5, 7, 10, 12, 21, 31, 34-35, 44; '654 claims 21, 24, 26, 35; '140 claim 30, 31, 34.	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a PCI bus transaction that has been serialized from a parallel form"	"[Peripheral Component Interconnect (PCI)/PCI] bus transaction": See above proposed construction of PCI Bus Transaction Terms. "a PCI bus transaction that has been serialized from a parallel form" for claim terms including "encoded," "serial," and "PCI bus transaction." Remaining portions of these phrases do not require construction, where the plain and ordinary meaning of "encoded" is "code representing [the recited bits of] a PCI bus transaction."

1. Claims reciting an "encoded" PCI bus transaction in a "serial [bit] stream" or "serial form" or "serially encoded"

The parties and Court agree that the *EMC Markman* construction, as specifically adopted by the Federal Circuit, applies to claim terms including "encoded," "serial," and "PCI bus transaction" and should be construed as "a PCI bus transaction that has been serialized from a parallel form." *See EMC Markman*, 2017 WL 6211051, at *5-8 (D. Mass. Dec. 8, 2017); *EMC Fed. Cir. Op.,* 2022 WL 1562847; *see also* Ex. 40, ACQIS P.R. 4-2 Preliminary Proposed Claim

Constructions, at 3; Ex. 41, *ACQIS LLC v. ASUSTek Computer, Inc.*, 6:20-cv-966-ADA, Dkt. 144.

2. Claims reciting a PCI bus transaction in a "serial form," "serial bit stream," or "conveyed serially"

As discussed in Section II above, ACQIS is precluded from arguing for a different construction of these terms. The absence of the word "encoded" from the claim limitation does not affect the Federal Circuit's construction because, as discussed below, none of ACQIS's IPR statements that formed the basis of the *EMC* Court's construction, and corresponding finding of disclaimer, were rooted in the word "encoded."[9] Indeed, the specifications describe converting a PCI bus transaction from a parallel to serial form separately from encoding a PCI bus transaction. *See* '750 Patent at 17:60-65, 18:9-12, 18:61-19:9, 19:23-30. Thus, the absence of "encoded" from the claim language does not affect the "serializ[ing]" aspect of the construction.

Even if the Court refuses to apply issue preclusion, as discussed above in Section II, Defendants' construction is the correct one because it is supported by the intrinsic evidence, and because it is the same construction adopted by the Federal Circuit in *EMC* for similar claim terms based on ACQIS's repeated statements to the PTAB. Indeed, Defendants' construction mirrors ACQIS's repeated characterizations that "one key to the invention was to serialize the otherwise parallel PCI bus transactions." Ex. 42, ACQIS '814 IPR Resp., at 3.

a. The Claims and Specification Require that a PCI Bus Transaction Be Converted to Serial Form.

All the asserted "PCI bus transaction" claims contain phrases that recite data of a "PCI bus transaction" that is conveyed "serially," in "serial form," or in a "serial bit stream." As discussed below, there is no dispute that a PCI bus transaction, when it is generated, is in a parallel form.

[9] Indeed, ACQIS's proposed construction of "encoded"—i.e., "code representing … a PCI bus transaction"—belies any significance to the term "encoded" as it relates to the *EMC* construction because it has nothing to do with "serializing," which was the focus of ACQIS's disclaimer.

The language of claims, requiring that a PCI bus transaction be in a "serial" form, therefore, compels Defendants' construction.

The specifications confirm the same, explaining that the claimed invention "relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel." '750 patent, at 3:21-24; 5:49-51. The specifications disclose that to use this interface, PCI bus transactions (which are in parallel form) are converted to serial form. This conversion is necessary because the interface channel uses serial channels whereas a PCI bus uses parallel lines. *Id*. at 6:43-47; *see also id.* at 5:49-51 ("The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel."); Ex. 43 (IPR2014-01462, Ex. 2021 (IPR Decl. of V. Lindenstruth)), ¶ 63 ("The PCI standard bus was a 32-bit wide parallel bus[.]").

To transmit parallel PCI bus transactions over the serial interface (i.e., applicant's XP Bus), the specification discloses how various elements of the PCI bus transaction—including all PCI address, data and control signals—are converted from parallel to serial form. *See, e.g.*, '750 patent, at 5:51-55; 17:60-62 ("***Encoders 1022 and 1023 format the PCI address/data bits*** to a form more suitable for ***parallel to serial conversion prior to transmittal on the XPBus***."); 18:61-19:15 ("The multiplexed ***parallel A/D bits and some control bits input to transmitter 1030 are serialized by parallel to serial converters 1032*** of transmitter 1030 into 10 bit packets."); 20:18-40; Figs. 10-11. After passing through the serial interface, the serialized form of the PCI transaction is converted back to a parallel form and decoded for use once again under the PCI protocol. *See, e.g.*, '750 patent, at 5:55-57 ("At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus."); 19:23-38 ("***Serial to parallel converters 1042 convert the serial bit packets received on lines PDR0 to***

PDR3 into parallel address/data and control bits ….”); 17:62-65; 18:42-47; 20:18-40; Figs. 7-8, 10-11. In short, a PCI bus transaction transmitted over a serial interface must undergo a parallel to serial conversion. There is simply no disclosure of sending PCI bus transaction data in serial form without first “serializing it from a parallel form.”

The Court should adopt Defendants’ construction given the unmistakable teachings of the specification and requirements of the claims.

b. ACQIS’s PTAB Statements Clearly and Unambiguously Stated that the Claimed Invention Requires Serialization of a Parallel PCI Bus Transaction.

ACQIS’s repeated statements before the PTAB to preserve validity of its patents constitute clear and unambiguous statements supporting Defendant’s construction. One district court has already found that disclaimer applies in this context:

> ACQIS repeatedly represented that “the whole point” of the invention is to convert a PCI bus transaction from parallel to serial and back to parallel. ACQIS’s argument was not only clear and unmistakable but also consistent throughout its briefing and oral argument. Each of the statements identified above reinforced ACQIS’s chosen metaphor of the hourglass, which, if nothing else, represents a PCI bus transaction beginning in parallel, converting to serial, and then back to parallel.

EMC Markman, 2017 WL 6211051, at *7. The Federal Circuit “specifically adopted” the district court’s constructions. *EMC Fed. Cir. Op*., 2022 WL 1562847, at *1.

ACQIS repeatedly and unequivocally characterized the heart of its claims as converting parallel PCI bus transactions to a serial form. ACQIS specifically argued “[a]s described in the specification . . . ***one key to the invention was to serialize the otherwise parallel PCI bus transactions*** to increase communication speeds for peripherals.” Ex. 44 (’873 IPR,[10] ACQIS Resp.) at 3; *see also id.* at 7 (“[T]he ‘873 claims are directed to a … architecture that permits faster

[10] The ’750, ’768, and ’797 patents asserted against Defendants are continuations of the ’873 patent.

PCI bus transactions with peripheral devices by ***serializing the PCI bus transaction***, including serializing the PCI transaction address. … The invention of the '873 patent … boost[s] speeds by making the PCI communication serial rather than parallel."). ACQIS also distinguished the prior art from the '873 patent on the basis that it did not perform this "key" serialization. *Id*. at 4 ("And Horst never used a serialized PCI bus transaction, only parallel."), 21-22 ("Horst never serializes any PCI bus transaction; even the peripheral-side PCI bus transaction . . . Horst teaches a different architecture and ***never serializes an actual PCI bus transaction***."); *see also* Ex. 42 ('814 IPR ACQIS Resp.) at 24 and 29 (distinguishing Horst for same reasons); *id.* at 4 ("Horst and Bogaerts … never used a serialized bus transaction, only parallel."), 43 (distinguishing Bogaerts prior art because it "never serializes an actual PCI bus transaction."); Ex. 36 (IPR Hr'g Tr.) at 46:23-24 ("The point about Horst is that Horst doesn't have a PCI transaction that is then serialized."). ACQIS's expert agreed that the claims require serialization of a PCI bus transaction. Ex. 39, Lindenstruth Dep. Tr. at 149:20-150:5 ("[Q.] [T]he claims … contemplate some sort of transformation of the PCI bus transaction into a format that is serially transmitted and then, on the other end, it would be converted back into PCI bus transaction format? [A.] … So yes."), 190:23-191:1 (explaining that the patents "are basically serializing the particular ongoing PCI transaction which is being then made parallel on the far end again").

This continued at oral argument. ACQIS repeatedly characterized its invention as an "hourglass" in which a PCI transaction in parallel form is converted into serial form for transmission over a serial channel and then converted from serial form back into parallel form. These statements were clear and unmistakable:

- "You have got a standard PCI bus, you have got the invention, depending on how you do it, but you have got the new bus in the center, and what that's doing is ***taking the parallel 32 bits coming down, putting them on a serial bus, moving them and then taking them back out. It's an hourglass***[.]" Ex. 36 (IPR Hr'g Tr.) at 39:21-40:2.

- "***The whole point is you start PCI***, whether you start here or down here, it makes no difference, whether it's the CPU or the printer. ***You start with the PCI address that's in this parallel slow form, serialize it and then take it back to the PCI form at the other end***." *Id*. at 31:25-32:4.
- "But the whole point of this invention and these claims is that they are centered around dealing with a standard. ***All of the computers out there have PCI . . . . And the point is you take it from parallel to serial and then back to parallel***." *Id.* at 34:14-18.
- "So I have created my PCI transaction . . . . And then I'm taking it at a parallel form, putting it into serial form and then back to parallel. … But the point is ***if you are trying to match it to the claims, you are taking a PCI transaction and serializing it***." *Id.* at 46:14-47:18.
- "Remember I said the hourglass, ***you start with the PCI, you got the parallel bits, serialize them, get them to the other side, push them back out***." *Id.* at 65:13-23.
- "I've got a PCI address, I have got it spelled out here, 32-bit word, and I take it, I put it on my serial line. So ***that's the whole point. I'm going from parallel, I'm putting on a serial line***." *Id*. at 30:21-24.
- "[W]hat the claim requires is that it is a ***PCI bus transaction***. That is defined by the standard. You know the three portions: Address, data, and control. … So I'm taking the transaction data, I don't think it matters where it originates from, then ***I'm going to take it, I'm going to serialize it*** and then send it out over my serial bus for speed purposes." *Id*. at 50:14-21.

Each of these statements show ACQIS unambiguously characterized the "whole point" of its claimed invention as serializing PCI bus transactions from a parallel to serial form. The Federal Circuit has long held that such statements are binding and limit the scope of the claims. *See Springs Window Fashions*, 323 F.3d at 994; *Aylus*, 856 F. 3d at 1362-64 (relying in part on patentee's statement that "'this is a key aspect of the claimed invention" in finding prosecution disclaimer).[11] Indeed, the Massachusetts *EMC* Court found disclaimer in construing similar claim terms, which were expressly adopted by the Federal Circuit. *See EMC Markman,* at *5-8; *EMC Fed. Cir. Op.*., 2022 WL 1562847, at *1. ACQIS's arguments, and the disclaimer based thereon, are based on the serialization of the PCI bus transaction from a parallel form, not encoding, which makes sense because as explained in the Asserted Patents, encoding by encoders 1022/1023 merely format the

[11] This applies to related patents as well. *Trading Techs. Int'l, Inc. v. Open E Cry, LLC*, 728 F.3d 1309, 1323 (Fed. Cir. 2013) ("prosecution history regarding a particular limitation in one patent is presumed to inform the later use of that same limitation in related patents").

address/data bits to a form "more suitable for parallel to serial conversion," but it is the parallel to serial converters 1032/1033 that actually perform the serialization that forms the basis for all of ACQIS's arguments before the PTAB. *See, e.g.*, '750 patent, at 17:60-62 and 18:61-67. The same result should follow here.

Accordingly, the Court should adopt Defendants' construction of claims reciting a PCI bus transaction in a "serial form," "serial form," or "conveyed serially" to mean "a PCI bus transaction that has been serialized from a parallel form."

F. "console"

'750 claims 5, 7, 10, 12, 24, 35, 44; '654 claims 20-21, 23; '140 claims 14-15, 17-19, 21, 31, 34.	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a chassis that connects several components of a computer system"	"a chassis or enclosure, housing one or more coupling sites, that connects components of a computer system"

In *Appro*, "console" was construed by the Eastern District of Texas as "a chassis that connects several components of the computer system," which ACQIS agreed to at the claim construction hearing. *ACQIS LLC v. Appro Int'l, Inc*., No. 6:09-cv-148, 2010 WL 3057371, at *5 (E.D. Tex. Aug. 2, 2010); *see also* '750 patent at 4:32-37; 10:55-67. ACQIS proposed this same construction in *Alcatel-Lucent*, which the Eastern District of Texas adopted, finding no reason to deviate from his prior construction. *EDTX Markman*, 2015 WL 1737853, at *7. In the case at hand, Defendants propose the same construction that ACQIS agreed to, and that the court adopted, in both prior cases. There is no valid reason to stray from this construction, which ACQIS has approved on two occasions. Defendants' construction should be adopted.

G. "USB" / "Universal Serial Bus (USB) protocol" / "Universal Serial Bus (USB) protocol data[/information]"

'797 patent: 33-34; '768 patent: 40; '750 patent: 7, 24; '654 patent: 20-21, 23; '140 patent: 15, 18-19, 21, 34, 36.

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard"	No construction necessary. These phrases should be given their plain and ordinary meaning.

The relevant meaning of the "USB" claim terms is their meaning when the inventor filed the earliest related patent application. *Fundamental Innovation,* 2018 WL 647734, at *11 (citation omitted) ("[T]he term 'USB' in the patents-in-suit should be limited to the Universal Serial Bus standards that existed at the time of the claimed invention."); *Uniloc*, 2021 WL 432183, at *8 (report and recommendation finding that terms "Bluetooth messaging" and "Bluetooth protocols" should be limited to functionality described in the Bluetooth Core Specification "as it existed at the time of the claimed invention").

As discussed above in Section III.A., the Asserted Patents trace back to patent applications filed on May 14, 1999 or May 12, 2000. Thus, the relevant meaning of the USB claim terms is the meaning they had as of May 12, 2000, at the latest. *Fundamental Innovation*, 2018 WL 647734, at *9 ("An invention cannot comply with standards not yet in existence.").

As of May 12, 2000, only USB versions 2.0 and earlier existed. Ex. 37 (Colwell Decl.), ¶¶ 40-41. Thus, a POSITA would have understood the patent's references to "USB," "Universal Serial Bus (USB) protocol" and "Universal Serial Bus (USB) protocol data/information" to mean version 2.0 and prior versions. *Id*. at ¶¶ 41-42.

The accuracy of Defendants' construction is confirmed by the fact that the three non-reissue Asserted Patents specifically reference USB 2.0. *See, e.g.*, '768 patent at 12:16-17. The Court in *ACQIS LLC v Samsung Electronics Co. LTD., et al.*, agreed with Defendants' proposed construction of the USB terms based on its review of the intrinsic evidence. Dkt. No. 92, *ACQIS LLC v Samsung Electronics Co. LTD., et al*., No. 2:20-cv-00295 (E.D. TX.) at 29-33.

ACQIS's "plain and ordinary meaning" constructions purportedly allow ACQIS to capture ***modern*** USB standards that are ***not*** disclosed in the Asserted Patents' specifications and that had ***not yet*** been developed. Ex. 37, ¶ 43. This is improper because a POSITA could not have understood the claims to encompass something that did not even exist until years after the invention. *Fundamental Innovation*, 2018 WL 647734, at *9-11 ("An invention cannot comply with standards not yet in existence."); *Uniloc*, 2021 WL 432183, at *8. Defendants' construction is consistent with the specification and the law, and should be adopted.

H. "serial bit channels" and "serial channel"

'750 claim 10, 12; '797 claims 33-34; '654 claims 20-21; '140 claims 14, 15, 17, 18, 19, 21, 30-31, 34-36, 38.	
Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
"a path on which units of information are transferred serially from one component to another"	No construction necessary. These terms should be given their plain and ordinary meaning. "serial": *See* proposed construction of "Serial" Terms above.

ACQIS agreed to Defendants' exact construction of these terms in front of Judge Davis. *EDTX Markman*, 2015 WL 1737853, at *3. This is because it is consistent with the intrinsic evidence. Specifically, each of the claims require that one or more "LVDS channel[s]" that comprise "two unidirectional, serial channels that transmit data in opposite directions" (or similar limitations). The claim language, therefore, contemplates that data is being transferred from one component to another. And the fact that it is a "serial channel" means that the data (or information) is being transferred "serially." As discussed herein, transmitting data in a serial form is a primary aspect of the invention. *See supra* Section III.E; *see also* '750 patent at 18:61-19:43, Title ("Computer system … that communicates serial bits of a peripheral component … in opposite directions"); '768 patent at Title (same). The specifications confirm that an "LVDS line" is a "bit based line … for transmitting serial bits" that uses a "serial data packet protocol." '750 patent at

25:1-5. A unidirectional LVDS line is used, for example, to serially transfer signals and bits from a host interface controller ("HIC") to a peripheral interface controller ("PIC"). *Id*. at 22:41-46; Fig. 15; *see also id*. at 4:47-54; 18:61-19:43; 24:26-45; Fig. 31. A different unidirectional line serially transmits signals and bits in the opposite direction, i.e., from the PIC to the HIC. *Id*. at 22:46-53; Fig. 15; *see also id*. at 4:47-54; 18:61-19:43; 24:26-45; Fig. 31. Accordingly, the Asserted Patents only disclose that a "serial bit channel" is a "path on which units of information are transferred serially from one component to another." There is no reason to depart from ACQIS's prior agreement. Defendants' construction should be adopted.

IV. UNDISPUTED CLAIM TERMS

A. "peripheral bridge" ('797 patent: 7; '768 patent: 4; '654 patent: 23, 26, 35)

The Parties agree "peripheral bridge" should be construed as "a component that interfaces with peripheral busses or peripheral devices."

V. CONCLUSION

Defendants respectfully request that the Court adopt their proposed claim constructions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure and Local Rule CV-5, I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via the Court's CM/ECF system on May 19, 2023.

/s/ *Mark C. Lang*
Mark C. Lang